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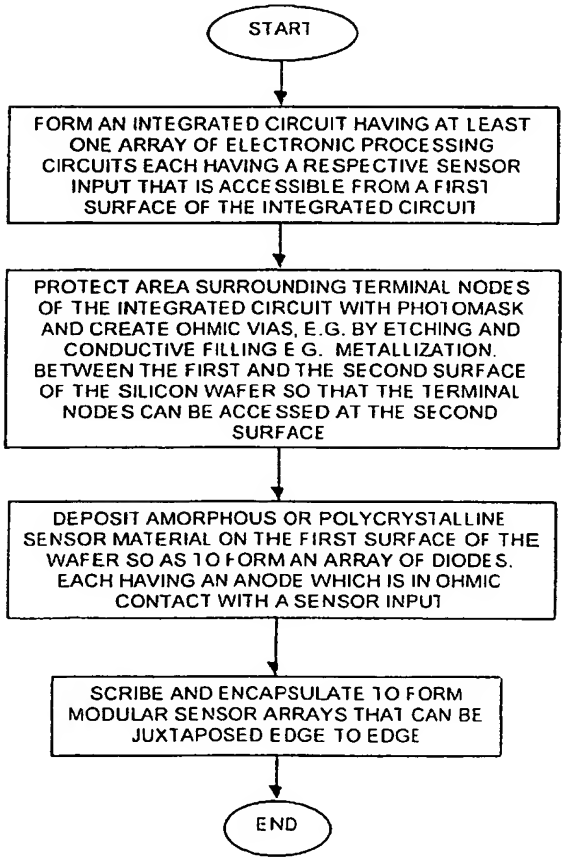
(54) Title: PIXEL SENSOR ARRAY AND METHOD OF MANUFACTURE THEREOF



(57) Abstract: A sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit is fabricated by first forming an integrated circuit having at least one array of electronic processing circuits (25, 26) each having a respective sensor input (24) disposed with terminal nodes of the integrated circuit toward a first surface of the wafer. In respect of either each pixel or each terminal node, an electrically conductive via (31) is formed through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface. This allows each electrically conductive via (31) exposed at the second surface of the wafer to serve for connection thereto of either a sensor element or a terminal connection that is electrically connected through the electrically conductive via (31) to the respective sensor input or terminal node.

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Pixel sensor array and method of manufacture thereof

FIELD OF THE INVENTION

This invention relates to pixel sensors for use in cameras, and in particular to such sensors as are used in nuclear and medical imaging systems.

BACKGROUND OF THE INVENTION

Pixel sensors are known to comprise an array of sensor elements such as diodes, and a complementary array of electronics, typically in the form of an ASIC and comprising a charge amplifier and processing electronics for each sensor element. In CCDs such as are used in miniature television cameras and the like, the sensor elements are formed of silicon diodes which are responsive to visible light for producing a current which is amplified by the charge amplifier and subsequently processed.

Pixel sensors for nuclear medical imaging are known that respond to high-energy photons such as X-rays or γ-rays and produce charge in a similar manner. Conventional silicon diodes are not suitable for such applications because they are transparent to the high-energy photons and therefore other materials such as cadmium telluride or mercury iodide are used instead. Since these materials are not based on silicon, the diode cannot be integrated together with the associated electronics as a single monolithic structure and this requires, in practice, that the sensor elements and the associated electronics be manufactured on separate wafers, which are then interconnected using bump bonding.

Fig. 1 shows pictorially a typical arrangement comprising a standalone 2-D pixel sensor depicted generally as 10 and comprising an upper sensor array 11 comprising multiple sensor elements (not shown), each of which is bump-bonded to a corresponding electronics module in a lower ASIC 12. In addition, power and control signals are fed to the sensor 10 and this typically requires that control-pads 13 be formed along at least one edge of the composite chip and which may be connected to external circuitry using wire-bonding 14.

The typical size of each pixel in such an array is 200 μm and the typical dimensions of the two-dimensional array is 1 cm^2. This means that there are typically some 625 pixels per pixel array. In practice, it is usually necessary to image over a much larger area, for example at least 10 x 10 cm^2. This requires that 100 pixel arrays must be packed together, for example as a 10 x 10 matrix. On the one hand, the bump bonding technique used in conventional pixel sensors militates against the closer packing density of the pixels so that it becomes difficult to increase the resolution of the sensor by packing more pixels into a pixel array, since the need to bump-bond each sensor to the corresponding electronics in a different array is a costly process and is subject to low yields. Furthermore, the provision of control-pads along an edge of each module and the need to wire bond these pads to external circuitry means that adjacent sensor arrays cannot be packed edge-to-edge without introducing a "dead" zone where there are, in fact, no pixels at all owing to the interposing I/O and control-pads. Moreover, the connection of the I/O control-pads to the external circuitry by wire bonding is also a costly and cumbersome process and further reduces the effective overall packing density.

EP 0415541 assigned to Shimadzu Corporation, published March 6, 1991 and entitled "*Semiconductor-based radiation image detector and its manufacturing method*" discloses a radiation image detector for detecting a radiation image with the image divided into pixels. The detector comprises a radiation-sensitive semi-conductor plate having a common bias electrode deposited on one surface thereof. A plurality of pixel-corresponding signal takeout electrodes are deposited on the other surface of the semiconductor plate, and a plurality of bumps are provided

each of which is fixed on a respective one of the signal takeout electrodes. A passivation film covers each signal takeout electrode where not in contact with its bump, and covering the clearances between the signal takeout electrodes. A base plate is provided with a plurality of contact pads corresponding to and in contact with the bumps.

SUMMARY OF THE INVENTION

It is thus an object of the invention to provide an improved low-cost pixel sensor, which is amenable to closer packing, obviates the above-mentioned drawbacks that are contingent on the use of bump-bonding and the provision of I/O control-pads and allows multiple sensor modules to be juxtaposed so as to form a larger area sensor without requiring any further manufacturing process after assembly.

These objects are realized in accordance with the invention by a method for fabricating a sensor array having a plurality of pixels each including a sensor element coupled to a sensor input of an electronic processing circuit, the method comprising:

integrating the electronic processing circuits on a wafer so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, providing an electrically conductive via through the wafer extending from either the respective sensor input or from the respective terminal node to a second surface of the wafer opposite the first surface;

thus allowing each electrically conductive via exposed at the second surface of the wafer to serve for connection thereto of either a sensor element or a terminal connection that is electrically connected through the electrically conductive via to the respective sensor input or terminal node.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to understand the invention and to see how it may be carried out in practice, a preferred embodiment will now be described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

Fig. 1 shows pictorially a typical prior-art pixel sensor assembly;

Fig. 2 shows pictorially a standard pixel ASIC that is mass-manufactured on a silicon wafer in a first manufacturing step according to the invention;

Fig. 3 shows pictorially the silicon wafer undergoing an optional second manufacturing step according to the invention;

Fig. 4 shows pictorially a third manufacturing step according to the invention;

Fig. 5 shows pictorially a fifth manufacturing step according to the invention for producing ohmic connections between each pixel input and a reverse side of the silicon wafer for allowing direct connection thereto of a pixel sensor;

Fig. 6 shows pictorially the reverse side of the silicon wafer including the multiple ohmic contacts produced according to the invention, each being associated with a respective sensor;

Fig. 7 shows pictorially a sixth manufacturing step according to the invention for depositing sensor material on the reverse side of the silicon wafer;

Fig. 8 shows pictorially a single sensor element according to the invention cut from the wafer shown in Fig. 7;

Figs. 9a and 9b show respectively pictorially top and side elevations of the pixel sensor of Fig. 8 mounted via bump-bonds to a ceramic board in a composite encapsulation having bump-bonds for mounting directly to a PCB motherboard without the need for wire-bonding;

Fig. 10 shows pictorially a two-dimensional array of encapsulated pixel sensors as shown in Fig. 9 mounted in side-to-side relationship so as to form a composite large array sensor;

Fig. 11 is a flow diagram summarizing the manufacturing process of a pixel sensor according to the invention;

Fig. 12 is a flow diagram summarizing alternative manufacturing processes of a pixel sensor according to the invention; and

Fig. 13 is a flow diagram summarizing an alternative manufacturing process of a pixel sensor according to the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Fig. 2 shows a silicon wafer 20 constituting an integrated circuit or chip, typically formed of a complementary metal oxide semiconductor (CMOS) wafer and being provided with scribe lines 21 so as to form a rectangular matrix of sensor elements 22 each of which, in turn, comprises a matrix of 3 x 5 pixels 23. The wafer 20 is processed at a silicon foundry in known manner and for the purpose of low-cost mass-production is processed according to the invention as an uncut wafer bearing multiple replicas of the same integrated circuit. Each pixel 23 includes a sensor input 24 that is connected to a charge amplifier 25 and a processing unit 26. The charge amplifier 25 together with the processing unit 26 constitute the pixel electronics to which the sensor element (not shown) is connected and which responds to a photon striking the sensor element for measuring the charge produced thereby. Thus, the silicon wafer 20 contains multiple replicas of the pixel array 22 which, after scribing, would produce multiple ASICs each containing an array of 3 x 5 pixel electronic circuits for connecting to a respective sensor element.

Optionally, the standard wafer 20 shown in Fig. 2 may be ground or etched so as to thin down the wafer from the reverse side 28 so as to remove the bulk of the silicon wafer 29, whereby the remainder of the wafer 20 is as thin as practically possible. It is also possible to use a pre-thinned wafer in the IC fabrication described above, in which case subsequent thinning is unnecessary. A pre-thinned wafer will, however, result in a higher manufacturing cost when mass-producing the pixel electronics.

In order to obviate the need for wire bonding as is used in hitherto proposed pixel sensors, the invention connects each sensor input 24 via a respective ohmic contact (or "via") through the silicon wafer to the reverse side thereof. This contact

may then be used to connect the sensor element directly to the sensor electronics by effectively bonding the sensor element in correct spatial disposition with respect to the electronics on the reverse side of the silicon wafer. This may be done in various ways, some of which will now be described.

Thus, referring to Fig. 4 the sensor element 24 is coated with extra photomask material 30, which effectively protects the area of the wafer surrounding the sensor input 24, whilst leaving the sensor input 24 itself exposed. It may also be necessary to produce a complementary photomask that covers the same region but is provided on the reverse side 28 of the silicon wafer in precise registration with the photomask that is disposed on the pixel 23. Once this is done, a connection may be formed to the sensor input 24 through the wafer by implanting the silicon wafer with an n-type donor impurity, being a pentavalent material such as antimony, phosphorus or arsenic to which the photomask 30 is impervious, so that the donor impurity penetrates only the sensor input 24 and creates a local increase in the conductivity of the silicon from the sensor input 24 through the wafer 20 to its reverse side, thus effectively forming a matrix of conductive vias 31, each of which connects a respective sensor input 24 to the reverse side of the wafer 20 as shown pictorially in Fig. 6.

An alternative approach is to provide a photomask on the reverse side only of the wafer that exposes the silicon in direct registration with the sensor input on the topside of the wafer and partially to etch holes through the wafer from the reverse side to the sensor input 24, whilst not etching all the way through the wafer. The resulting bores are then filled with conductive material such as aluminum.

Yet another possibility is to combine the two above-mentioned approaches whereby holes are partially etched through the wafer from the reverse side and a p-type impurity, such as boron, is implanted from the top side so as to render the wafer directly underneath each sensor input conductive. The partial bores are then filled with conductive material such as aluminum, which abuts the now-conductive wafer and completes the ohmic contact to the reverse side of the wafer.

Referring to Fig. 7 there is shown a subsequent stage in the manufacturing process where desired amorphous or polycrystalline sensor material such as mercury iodide is grown on the top side of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respect one of the conductive vias 31 (shown in Fig. 6) and such that the opposite, exposed, surface of the sensor material forms a common cathode towards which incident photons are directed. Thus, Fig. 7 shows pictorially a composite wafer 35 having a lower silicon wafer 36 as described above, on top of which is grown an amorphous or polycrystalline sensor material 37 so as to form a matrix of sensor elements having a common cathode constituted by the upper surface of the device and a respective anode (not shown) that is effectively sandwiched between the upper sensor layer 37 and the lower silicon wafer 36 and is connected via a corresponding one of the vias formed in the silicon wafer 36.

As shown in Fig. 8, the wafer 35 is now scribed along the scribe lines so as to produce individual sensor chips 40, which in the specific example shown in the figure comprises 5 x 3 pixel elements in a two-layer structure having an upper layer 41 formed of a silicon wafer and having integrated therewith pixel electronics reference 23 in Fig. 4 and having a lower layer 42 on which the sensor elements themselves are deposited. Toward the upper layer 41 are also formed terminal nodes to allow for the external connection to the pixel electronics of power, I/O and control connections. This is typically done by means of terminal pads 43, which are metallized on the outer surface of the silicon wafer in known manner and formed already in an earlier stage of the fabrication corresponding to the silicon wafer 20 shown in Fig. 2. In use, access to an individual pixel in the sensor array is achieved by addressing the required pixel and the location of an active pixel in the sensor array is likewise determined by decoding its address. In a sensor array having, for example, 1024 pixels the required address bus has 10 lines and in general the required address bus for a pixel array having N pixels has $\log_2 N$ lines. Thus far fewer terminal nodes are required than sensor inputs.

As explained above, pixel sensors are deposited on the lower layer 42, whose outer surface constitutes a common cathode such that the anodes of each sensor element are connected to a corresponding sensor input of the pixel electronics via a corresponding through-connect or via formed through the body of the silicon wafer 41. Likewise, the terminal pads 43 are formed on the outer surface of the silicon layer 41 rather than being brought to edge connections as is typically done in hitherto-proposed configurations. This greatly facilitates mounting of the pixel array and allows multiple pixel arrays to be cascaded in edge-to-edge relationship, resulting in a much more compact configuration with greatly reduced dead space compared to hitherto-proposed configurations.

Figs. 9a and 9b show how the pixel sensor module 40 shown in Fig. 8 may be encapsulated so that the common cathode of the pixel sensor layer 42 is uppermost and the terminal pads 43 are connected via bump-bonds 45 to a ceramic board 46 which are low density and easy to manufacture. The ceramic board 46 feeds bump-connections 47 through to surface mounted pins or bores (e.g., PGA or BGA standard). The complete arrangement is encapsulated so as to form a module 48 that is easily mounted on to a PCB motherboard. The module 48 is very easy to handle and can be mounted as one of many identical elements that are mounted edge-to-edge so as to form a two-sensor having a much larger surface area and minimum dead space as shown pictorially in Fig. 10 where a large sensor array 50 is formed by mounting multiple sensor modules 48 in edge-to-edge arrangement, all surface mounted to a standard PCB assuming that BGA encapsulation is employed. If, alternatively, PGA encapsulation were employed, then the modules 48 would typically be mounted in IC sockets.

It is obviously important that the vias are not short-circuited by the silicon wafer 20. This might conceivably occur, for example, if the vias are filled with metal since the junction of the metal vias with the bulk silicon could form a Schottky diode. During actual use of the sensor, such a Schottky diode could become reverse biased and conduct, thus creating a short-circuit between the vias.

In order to militate against the possibility of conduction between the vias through the bulk of the silicon wafer, the integrity of the insulation between the vias in the silicon wafer it must be ensured. To this end, the insulating properties of the silicon wafer can be enhanced by suitable choice of the silicon wafer. Generally, it will always be a type of which the surface (first surface) is prepared in a standard manner for IC (e.g. CMOS) manufacturing. However, the bulk material can be varied so as to provide better insulation properties. Typical variations are:

1. Standard bulk silicon substrate (homogenous all the way through). This would be the "normal" choice.
2. Silicon on Insulator (SoI) substrate.
3. Epitaxial layer silicon substrate.

It will be apparent that modifications may be made to the assembly without departing from the scope of the invention as claimed which resides, principally, in the provision of ohmic connections that are formed in the silicon wafer so as to allow ohmic connection therethrough of a pixel sensor element to the input connection of the corresponding pixel electronics that is integrated into the silicon wafer on the top side thereof. By such means, the need to interconnect each sensor element to the corresponding electronics in the silicon wafer via bump-connections is avoided thus allowing a much more compact assembly to be produced. Furthermore, since the I/O and controls pads may easily be mounted on the top surface of the silicon, this obviates the need to provide connections along the edge of the pixel assembly, thus rendering the assembly still more compact and allowing easy expansion of the pixel array by mounting multiple modules edge-to-edge with minimum intervening dead space.

Fig. 11 is a flow diagram summarizing the essential features of the above-described manufacturing process of a pixel sensor according to the invention, wherein the sensor material is deposited on the second surface of the wafer and the sensor elements are electrically connected through the electrically conductive vias (31) to the respective sensor inputs.

Whilst, in the preferred embodiment as described above, the sensor elements are themselves deposited using mercury iodide on to the silicon wafer, it will be appreciated that other materials may be used such as cadmium zinc telluride and cadmium mercury iodide. Likewise, the invention contemplates providing the sensor elements as a completely separate integrated unit, whose multiple sensor elements may each be connected to a respective pixel electronics unit in the silicon layer via the ohmic contact formed therethrough according to the invention. Thus the invention also contemplates the situation where the sensor elements and the sensor electronics are formed in discrete layers, which are bonded together rather than being formed as a monolithic structure.

Furthermore, while a preferred embodiment has been described with regard to CMOS circuitry, it will be appreciated that the principles of the invention are applicable to other technologies.

Although use of such sensors in nuclear and medical imaging systems has been mentioned, it is to be noted that the invention is not limited to any particular application. Thus, other applications of the invention will be apparent to one skilled in the art and include, without limitation, X-ray computed tomography; night vision sensors; standard medical and industrial X-ray devices; nuclear medicine PET/SPECT sensors; particle detectors; X-ray diffraction detectors and others.

It should also be noted that in the fabrication stage shown in Fig. 8, the wafer does not need to be divided along every scribe line. Thus, in the example described in the preferred embodiment where each pixel sensor comprises an array of 3 x 5 pixels, a larger array of 6 x 5 pixels can be fabricated simply by not scribing between two adjacent pixel arrays. Likewise, an array of 6 x 10 pixels can be formed by suitable division of the wafer 20. In saying this, it is of course to be noted that the invention is not limited to any specific number or arrangement of pixels in each pixel array and the usual cost/yield considerations apply. Thus, by reducing the number of pixels in each array, fewer pixels are wasted upon discarding faulty pixel arrays. Theoretically, one large pixel array could be formed

using the complete area of the wafer; but in this case a fault in a single pixel would require that the complete wafer be discarded.

In the preferred embodiment, the electronic processing circuits include amplifiers and further processing circuitry. This allows incident photons to trickle charge the pixel array and to be counted on impact. However, this also is not intended to limit the invention since at their most basic the electronic processing circuits can be simply capacitors that store the incoming charge, in a manner somewhat analogous to a CCD, where charge is read out sequentially similar to a shift register.

In the embodiments so far described, the sensor inputs together with terminal nodes are formed toward a first surface of the CMOS wafer and the sensor elements are either deposited on the opposite, second surface or otherwise fixed thereto in exact registration with the sensors inputs on the first surface. This results in the sensors inputs and the sensor elements themselves being disposed on opposite surfaces of the wafer and ohmic connection between them is achieved by means of electrically conductive vias that extend through the wafer. In such case, the terminal nodes must be accessible from the first surface of the CMOS wafer opposite the sensor elements so as to allow external connection thereto. This requires that the insulating silicon oxide layer covering the terminal nodes be removed so as expose the terminal nodes. External connection may then be achieved via terminal pads metallized on the first surface of the wafer in electrical contact with the exposed terminal nodes or directly on to the exposed vias.

However, the same principle may be used in reverse, whereby the terminal nodes are effectively dislocated by means of electrically conductive vias to an opposite surface of the wafer. This allows the sensor material to be deposited directly on the same surface of the wafer as the sensor inputs, thus obviating the need in this case for electrically conductive vias to be formed for these routing these connections to an opposite surface of the wafer. In other words, the sensor elements and the connections to the terminal nodes are always disposed on opposite surfaces of the wafer, although the sensor inputs and the terminal nodes are formed

on the same surface. In the first case, as described above with reference to Figs. 1 to 11, where the sensor elements are deposited on the second surface of the wafer, they are connected to the sensor inputs by respective electrically conductive vias and access to the terminal nodes is provided from the first surface for allowing direct connection thereto, for example by terminal pads. In the second case, the sensor elements are deposited directly on the same surface as the sensor inputs. In this case, the terminal nodes are connected by respective electrically conductive vias to the opposite surface of the wafer, where the actual terminal pads may be formed, or other connection to the now dislocated terminal nodes may be ensured. Access to the terminal nodes from the first surface of the wafer is, in this case, prevented since otherwise the sensor elements would short-circuit the terminal nodes. Such short-circuiting is avoided by the silicon dioxide insulating layer that covers the terminal nodes before the sensor elements are deposited.

In this context, it is to be noted that in CMOS technology, the CMOS layer is covered by an insulating layer of silicon oxide, which must be removed if a circuit element is to be exposed in order to allow actual electrical connection thereto. Thus, in the first case where the sensor elements are deposited on the second surface of the wafer, the terminal nodes are exposed and metallized on the first surface. In the second case, where the sensor elements are deposited on the first surface of the wafer, the sensor inputs are exposed to allow electrical connection of the sensor elements. In this case, the terminal nodes are ohmically coupled to the second surface of the wafer by the electrically conductive vias and terminal connections thereto may be formed either by means of terminal pads or by direct connection to the ohmic diffusions of the vias. Thus, in both cases the sensor inputs and the terminal nodes are formed toward the first surface of the wafer, although depending on the circuit topology, access may be denied thereto by the silicon oxide insulation layer.

It should be noted that terminal nodes may be formed in the sensor chip for allowing any required external connection.

It should also be noted that the invention contemplates other approaches for depositing the electrically conductive vias than the specific process described above with reference to Fig. 11. For example, prior to sending the wafer to the CMOS foundry for fabricating the pixels 23 comprising the sensor electronics shown in Fig. 4, the electrically conductive vias may be pre-formed in the native silicon wafer.

Fig. 12 is a flow diagram summarizing the principal operations carried out in such a method of fabrication in accordance with various embodiments. Thus, according to a first embodiment, sensor material is deposited on the second surface of the wafer so as to form the basis for an array of diodes. The thus exposed surface of the sensor material will form a common cathode on to which incident radiation will impinge. The anodes will abut the wafer, but are only realized when actual connections are made thereto by the electrically conductive vias that will connect them to the sensor electronics, when this is eventually formed. Electrically conductive vias are formed in the native silicon wafer using any of the techniques described above. Thus, as shown in Fig. 12, areas of the native wafer that are to be protected may be covered with photomask and the vias created by etching and conductive filling e.g. metallization through the wafer. Once this is done, the points of contact of the respective vias with the sensor material form the respective anodes of the sensor elements or pixels. The pre-processed silicon wafer is now sent to the CMOS foundry where the pixels 23 are formed in normal manner so that either the sensor inputs or the terminal nodes are in exact registration with the vias, depending on whether the sensor material is to be deposited on the opposite surface of the same surface of the pixels 23, as explained above. In either case, at the end of the process the terminal nodes and the sensor material are deposited on opposite surfaces of the wafer and either the sensors are connected to their respective sensor inputs by means of the pre-formed electrically conductive vias or, alternatively, the terminal pads are connected to their respective terminal nodes by means of the electrically conductive vias. As noted above, the connections to the terminal nodes

need not be via metallized pads, since direct connection to the ohmic diffusion may be made if required.

In an alternative method, the electrically conductive vias are formed first in the native wafer as explained above. The sensor material is then deposited on the second surface of the wafer so as to form the basis for an array of diodes. As explained above, the thus exposed surface of the sensor material will form a common cathode on to which incident radiation will impinge. The anodes will abut the wafer at the respective points of contact with the already-formed vias, but are only realized when actually connections are made thereto by the sensor electronics, which is now formed at the CMOS foundry.

According to a third approach, the electrically conductive vias are formed first in the native wafer as explained above. The processing electronics is now formed at the CMOS foundry in precise registration with the electrically conductive vias. The sensor material is then deposited on the second surface of the wafer so as to form an array of diodes. The exposed surface of the sensor material forms a common cathode on to which incident radiation will impinge. The anodes abut the wafer at the respective points of contact with the already-formed vias, which are connected to the sensor electronics.

Fig. 13 is a flow diagram summarizing the essential features of the above-described manufacturing process of a pixel sensor according to the invention, wherein the sensor material is deposited on the first surface of the wafer and the terminal pads are electrically connected through the electrically conductive vias to the respective terminal nodes. Although in Fig. 13 only one manufacturing approach is shown, it will be appreciated that any one of the approaches described above with reference to Fig. 12 may be employed also in the case where the terminal pads are electrically connected to the terminal nodes through respective electrically conductive vias.

In all cases, after the wafer is processed it is scribed and encapsulated to form modular sensor arrays that can be juxtaposed edge to edge.

The invention has been described with particular reference to two distinct configurations: one where the sensor inputs are dislocated from the first surface to the second surface; and the second where the terminal nodes are dislocated from the first surface to the second surface. These configurations have been described as being what is currently believed to be of most practical importance. But it is clear that the teachings of the invention would allow hybrid configurations also, where for example the sensor inputs are dislocated as well as specific ones of the terminal nodes. Thus, in the appended claims the provision of an electrically conductive via in respect of either each pixel or each terminal node is not intended to preclude the possibility of providing an electrically conductive via in respect of each pixel and some of the terminal nodes.

CLAIMS:

1. A method for fabricating a sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit, the method comprising:

integrating the electronic processing circuits (25, 26) on a wafer (20) so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input (24) and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, providing an electrically conductive via (31) through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface;

thus allowing each electrically conductive via (31) exposed at the second surface of the wafer to serve for connection thereto of either a sensor element or a terminal connection that is electrically connected through the electrically conductive via (31) to the respective sensor input or terminal node.

2. The method according to Claim 1, wherein the electrically conductive vias serve to connect respective sensor elements to respective sensor inputs and there is further included:

growing the sensor elements on the second surface of the integrated circuit, each in registration with a corresponding one of the electrically conductive vias.

3. The method according to Claim 1, wherein the electrically conductive vias serve to connect respective terminal pads to respective terminal nodes and there is further included:

growing the sensor elements on the first surface of the integrated circuit, with the terminal nodes in registration with respective electrically conductive vias.

4. The method according to any one of Claims 1 to 3, wherein the integrated circuit includes multiple arrays of pixels and there is further included:

dividing the integrated circuit into discrete sensor arrays.

5. The method according to any one of Claims 1 to 4, further including:

assembling multiple sensor arrays edge to edge so as to form a composite sensor array having an extended surface area.

6. The method according to any one of Claims 1 to 5, further including:

thinning down the wafer (29) from a reverse side (28) thereof so as to remove the bulk of the wafer.

7. The method according to any one of Claims 1 to 5, wherein the wafer (20) is pre-thinned prior to providing the electrically conductive vias (31) through the wafer (20).

8. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding the sensor inputs or the terminal nodes (24), whilst leaving the sensor inputs or the terminal nodes (24) exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only the sensor inputs (24) or the terminal nodes and creates a local increase in the conductivity of the wafer from the sensor inputs (24) or the terminal nodes through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31), each of which connects a respective sensor input (24) or terminal node to the second surface of the wafer (20).

9. The method according to Claim 8, further including:

producing a complementary photomask that covers said area of the wafer on the second surface thereof and is in precise registration with the photomask (30) that is disposed on the first surface thereof.

10. The method according to Claim 8 or 9, wherein the wafer is based on silicon and said material is a p-type impurity.

11. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with the sensor inputs or the terminal nodes on the first surface of the wafer,

etching holes through the wafer from the second surface to the sensor inputs or to the terminal nodes (24), whilst not etching all the way through the wafer so as to form bores, and

filling the bores with conductive material.

12. The method according to any one of Claims 1 to 7, wherein providing electrically conductive vias (31) through the wafer (20) includes:

partially etching holes through the wafer from the second surface so as to form partial bores,

implanting the wafer from the first surface thereof with a material to which the photomask (30) is impervious, so that said material penetrates only the sensor input (24) or the terminal node and renders the wafer conductive directly abutting each sensor input or terminal node, and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

13. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding an intended location of each sensor input or terminal node (24), whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each sensor input (24) or terminal node through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31) through the wafer (20).

14. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

coating the first surface of the wafer (20) with photomask (30) for protecting an area surrounding an intended location of each sensor input or terminal node (24), whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask (30) is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each sensor input (24) or terminal node through the wafer (20) to the second surface thereof, thus forming a matrix of conductive vias (31) through the wafer (20).

15. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing circuits by:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with respective locations on the first surface of the wafer of intended sensor inputs or terminal nodes,

etching holes through the wafer from the second surface to said locations (24), whilst not etching all the way through the wafer so as to form bores, and

filling the bores with conductive material.

16. The method according to any one of Claims 1 to 7, wherein the electrically conductive vias (31) are formed in the wafer (20) prior to formation of the processing electronics by:

partially etching holes through the wafer from the second surface so as to form partial bores,

implanting the wafer from the first surface thereof with a material to which the photomask (30) is impervious, so that said material penetrates only the intended sensor input (24) or the intended terminal node and renders the wafer conductive directly abutting each intended sensor input or terminal node, and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

17. The method according to any one of Claims 1 to 16, wherein the electrically conductive vias (31) serve to connect respective sensor elements to respective sensor inputs and there is further included:

growing amorphous or polycrystalline sensor material on the second surface of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respective one of the conductive vias (31) and such that the first surface of the sensor material forms a common cathode.

18. The method according to any one of Claims 1 to 12, wherein the electrically conductive vias (31) serve to connect respective terminal connections to respective terminal nodes and there is further included:

growing amorphous or polycrystalline sensor material on the first surface of the wafer so as to form an array of diodes, each having an anode which is in ohmic contact with a respective one of the sensor inputs and such that the second surface of the sensor material forms a common cathode, and

forming on the second surface of the wafer a plurality of metallized terminal pads each in ohmic contact with a respective one of the electrically conductive vias.

19. The method according to any one of Claims 13 to 18, wherein the sensor material and the terminal connections are formed on the wafer (20) prior to formation of the processing circuits (25, 26).

20. The method according to any one of Claims 1 to 19, wherein the integrated circuit includes multiple arrays of electronic processing circuits (25, 26) separated by scribe lines and there is further included:

scribing along the scribe lines so as to produce individual sensor chips (40).

21. The method according to any one of Claims 1 to 20, further including:

connecting terminal pads (43) metallized on an outer surface of the wafer via bump-bonds (45) to a ceramic board (46) that feeds bump-connections (47) through to surface mounted pins or bores, and

encapsulating so as to form a module (48).

22. The method according to Claim 21, further including:

mounting several of said modules (48) edge to edge so as to form a two-dimensional sensor (50) of larger surface area than a single module.

23. A sensor array or module manufactured according to any one of Claims 1 to 22.

24. A sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit, the sensor array comprising:

a wafer having integrated therein the electronic processing circuits (25, 26) so as to form an integrated circuit having at least one array of electronic processing circuits (25, 26) each electronic processing circuit having a respective sensor input (24) and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, an electrically conductive via (31) through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface and serving for electrical connection of either a respective sensor element or a respective terminal connection through the respective electrically conductive via (31) to the respective sensor input or terminal node.

AMENDED CLAIMS

[received by the International Bureau on 2nd September 2003 (02.09.03) ; original claims 23 and 24 replaced by original claims 24 and 25 ; new claims 23 and 26 added ; remaining claims unchanged]

22. The method according to Claim 21, further including:

mounting several of said modules (48) edge to edge so as to form a two-dimensional sensor (50) of larger surface area than a single module.

23. The method according to any one of the preceding claims, when used to fabricate a sensor array for a high energy photon imaging detector.

24. A sensor array or module manufactured according to any one of Claims 1 to 23.

25. A sensor array having a plurality of pixels each including a sensor element coupled to a sensor input (24) of an electronic processing circuit, the sensor array comprising:

a wafer having integrated therein the electronic processing circuits (25, 26) so as to form an integrated circuit having at least one array of electronic processing circuits (25, 26) each electronic processing circuit having a respective sensor input (24) and the integrated circuit having a plurality of terminal nodes, the sensor inputs and the terminal nodes being disposed toward a first surface of the wafer, and

in respect of either each pixel or each terminal node, an electrically conductive via (31) through the wafer (20) extending from either the respective sensor input (24) or from the respective terminal node to a second surface (28) of the wafer opposite the first surface and serving for electrical connection of either a respective sensor element or a respective terminal connection through the respective electrically conductive via (31) to the respective sensor input or terminal node.

26. The sensor array according to Claim 25, being configured for use in a high energy photon imaging detector.

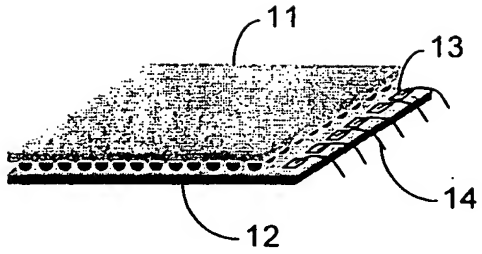

FIG. 1

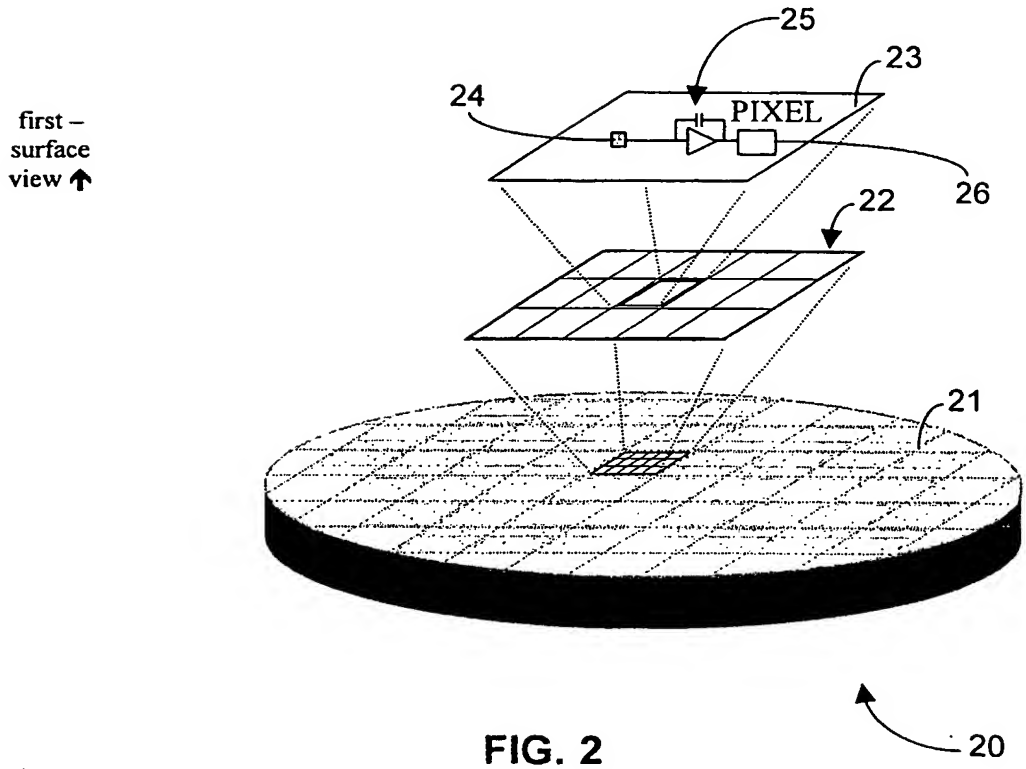

FIG. 2

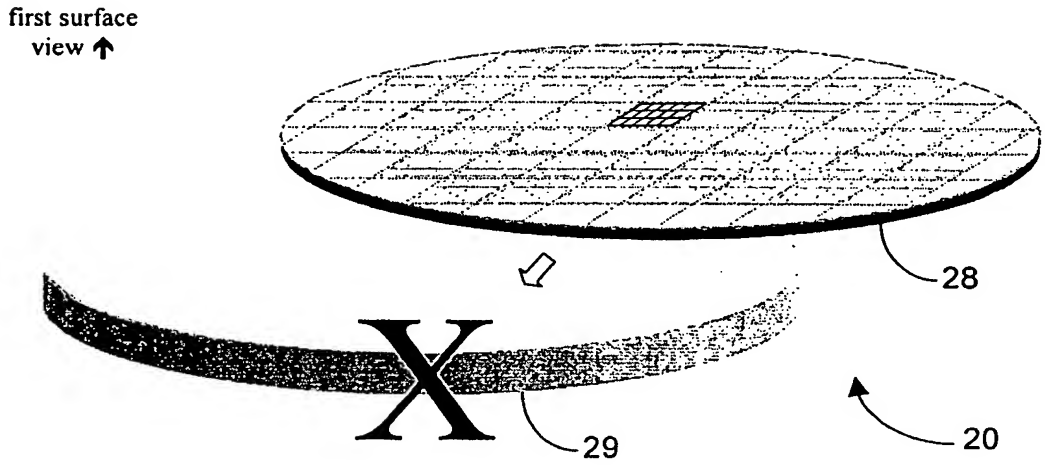
first surface
view
28
X
29
20

FIG. 3

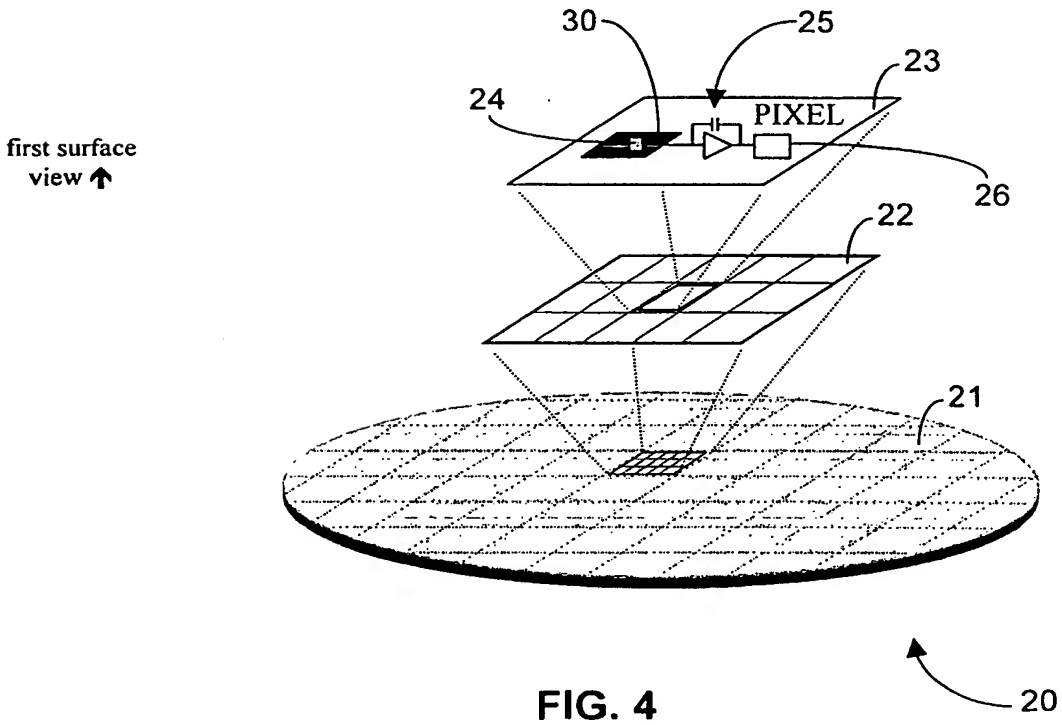
30
25
23
24
PIXEL
26
22
21
first surface
view
20

FIG. 4

first surface view ↑

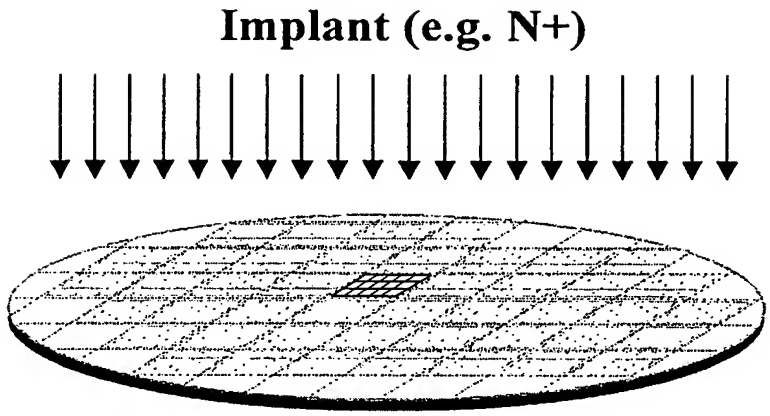

FIG. 5

second surface view ↓

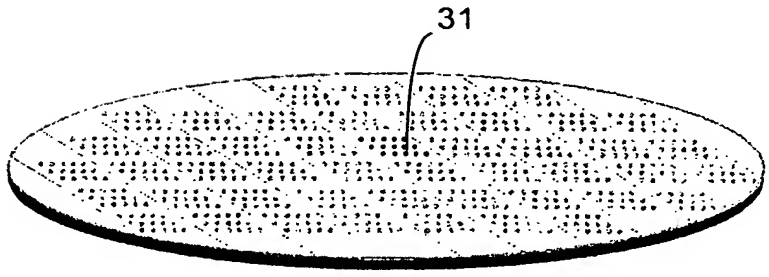

FIG. 6

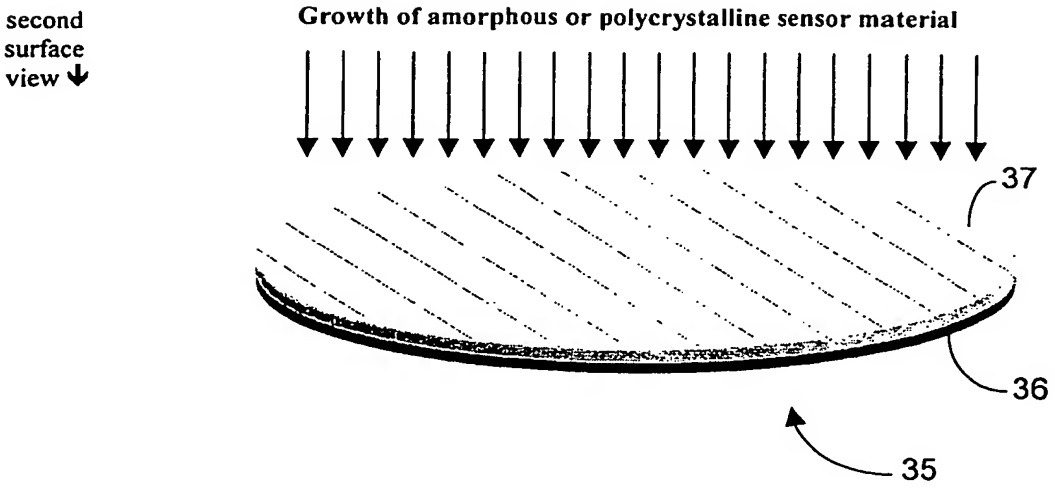
second
surface
view
Growth of amorphous or polycrystalline sensor material
37
36
35

FIG. 7

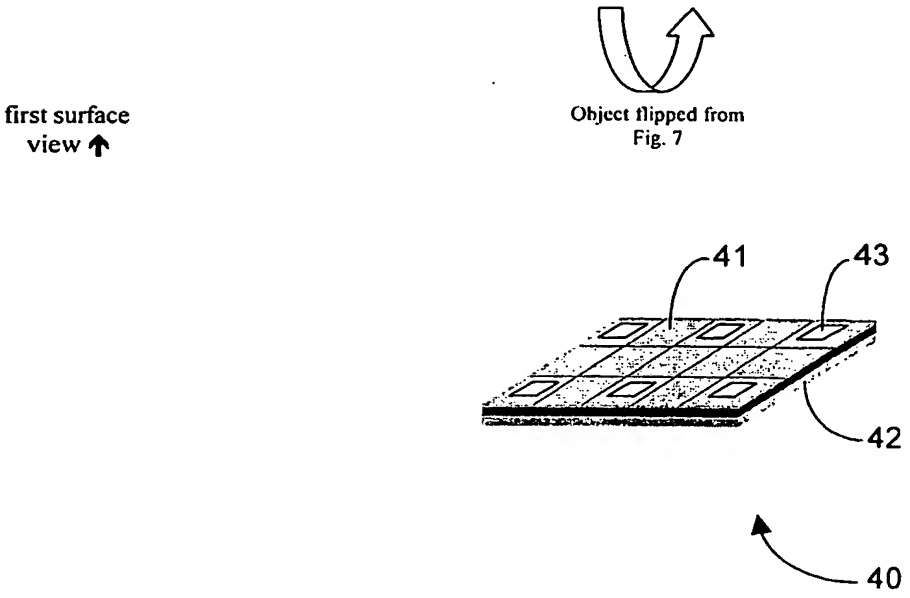
first surface
view
Object flipped from
Fig. 7
41
43
42
40

FIG. 8

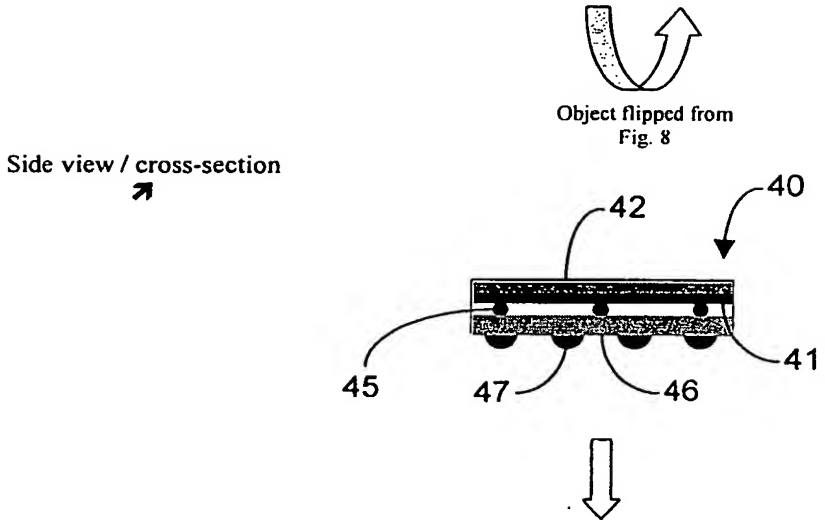

FIG. 9a

FIG. 9b

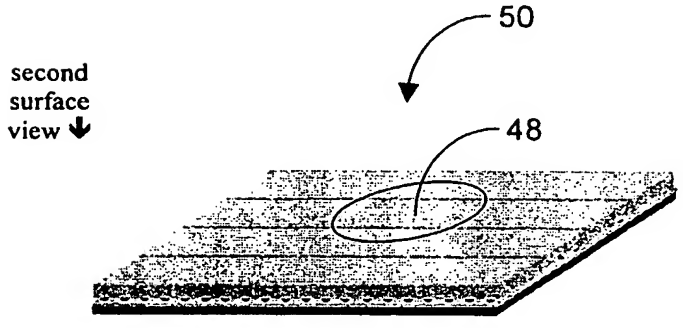

FIG. 10

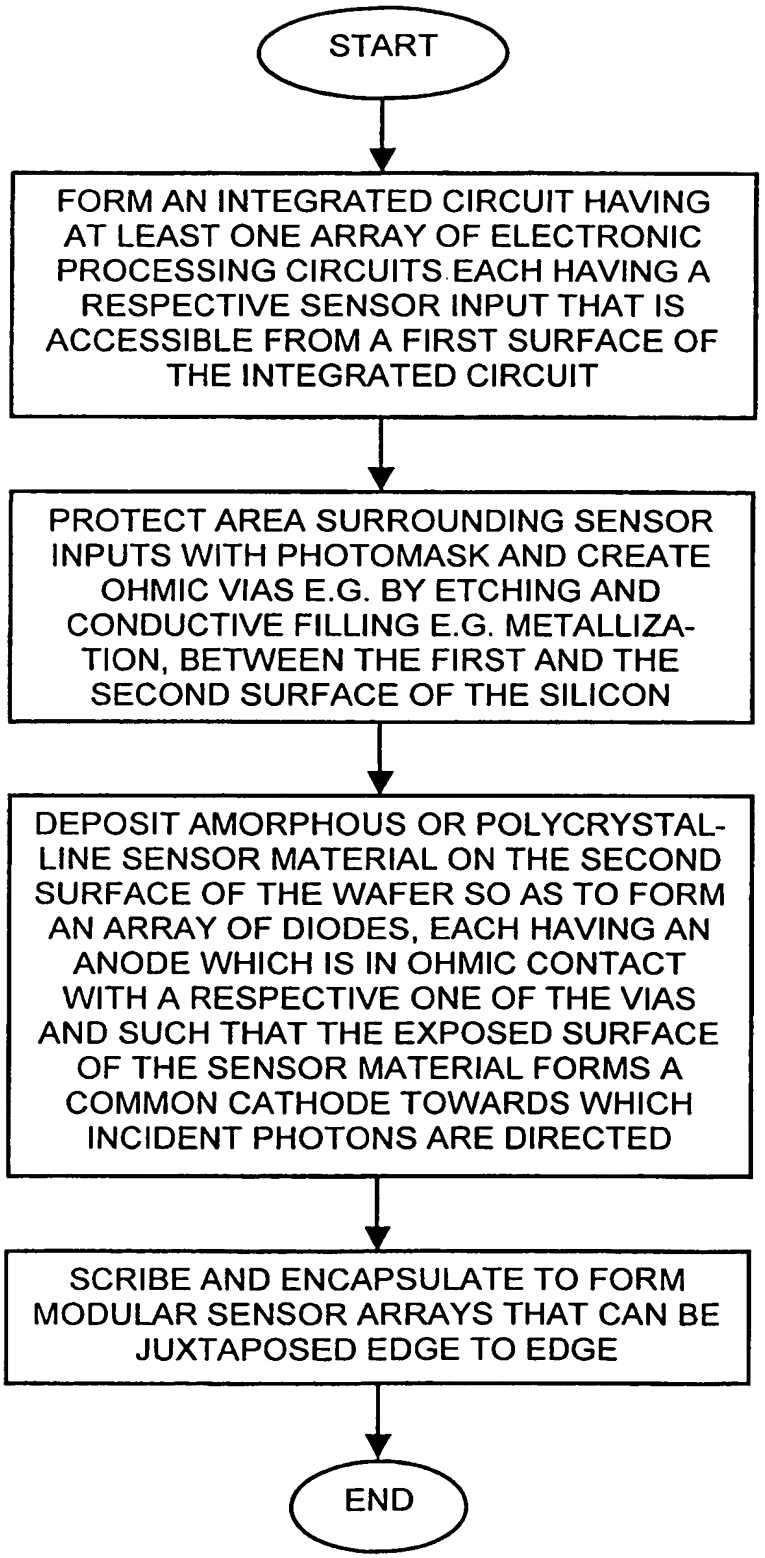
START
FORM AN INTEGRATED CIRCUIT HAVING AT LEAST ONE ARRAY OF ELECTRONIC PROCESSING CIRCUITS EACH HAVING A RESPECTIVE SENSOR INPUT THAT IS ACCESSIBLE FROM A FIRST SURFACE OF THE INTEGRATED CIRCUIT
PROTECT AREA SURROUNDING SENSOR INPUTS WITH PHOTOMASK AND CREATE OHMIC VIAS E.G. BY ETCHING AND CONDUCTIVE FILLING E.G. METALLIZATION, BETWEEN THE FIRST AND THE SECOND SURFACE OF THE SILICON
DEPOSIT AMORPHOUS OR POLYCRYSTALLINE SENSOR MATERIAL ON THE SECOND SURFACE OF THE WAFER SO AS TO FORM AN ARRAY OF DIODES, EACH HAVING AN ANODE WHICH IS IN OHMIC CONTACT WITH A RESPECTIVE ONE OF THE VIAS AND SUCH THAT THE EXPOSED SURFACE OF THE SENSOR MATERIAL FORMS A COMMON CATHODE TOWARDS WHICH INCIDENT PHOTONS ARE DIRECTED
SCRIBE AND ENCAPSULATE TO FORM MODULAR SENSOR ARRAYS THAT CAN BE JUXTAPOSED EDGE TO EDGE
END

FIG. 11

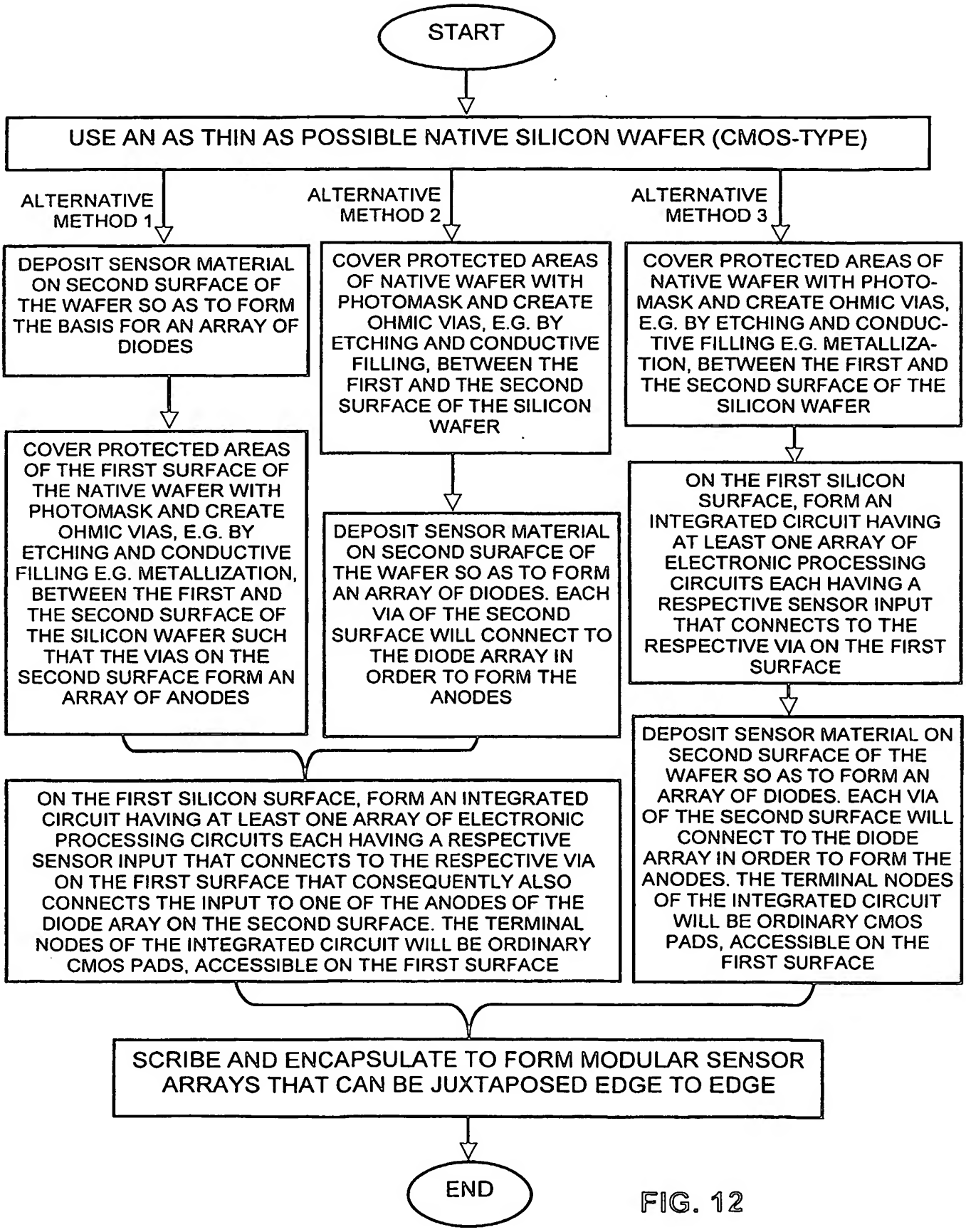
START
USE AN AS THIN AS POSSIBLE NATIVE SILICON WAFER (CMOS-TYPE)
ALTERNATIVE METHOD 1
ALTERNATIVE METHOD 2
ALTERNATIVE METHOD 3
DEPOSIT SENSOR MATERIAL ON SECOND SURFACE OF THE WAFER SO AS TO FORM THE BASIS FOR AN ARRAY OF DIODES
COVER PROTECTED AREAS OF NATIVE WAFER WITH PHOTOMASK AND CREATE OHMIC VIAS, E.G. BY ETCHING AND CONDUCTIVE FILLING, BETWEEN THE FIRST AND THE SECOND SURFACE OF THE SILICON WAFER
COVER PROTECTED AREAS OF NATIVE WAFER WITH PHOTO-MASK AND CREATE OHMIC VIAS, E.G. BY ETCHING AND CONDUC-TIVE FILLING E.G. METALLIZA-TION, BETWEEN THE FIRST AND THE SECOND SURFACE OF THE SILICON WAFER
COVER PROTECTED AREAS OF THE FIRST SURFACE OF THE NATIVE WAFER WITH PHOTOMASK AND CREATE OHMIC VIAS, E.G. BY ETCHING AND CONDUCTIVE FILLING E.G. METALLIZATION, BETWEEN THE FIRST AND THE SECOND SURFACE OF THE SILICON WAFER SUCH THAT THE VIAS ON THE SECOND SURFACE FORM AN ARRAY OF ANODES
DEPOSIT SENSOR MATERIAL ON SECOND SURAFCE OF THE WAFER SO AS TO FORM AN ARRAY OF DIODES. EACH VIA OF THE SECOND SURFACE WILL CONNECT TO THE DIODE ARRAY IN ORDER TO FORM THE ANODES
ON THE FIRST SILICON SURFACE, FORM AN INTEGRATED CIRCUIT HAVING AT LEAST ONE ARRAY OF ELECTRONIC PROCESSING CIRCUITS EACH HAVING A RESPECTIVE SENSOR INPUT THAT CONNECTS TO THE RESPECTIVE VIA ON THE FIRST SURFACE
ON THE FIRST SILICON SURFACE, FORM AN INTEGRATED CIRCUIT HAVING AT LEAST ONE ARRAY OF ELECTRONIC PROCESSING CIRCUITS EACH HAVING A RESPECTIVE SENSOR INPUT THAT CONNECTS TO THE RESPECTIVE VIA ON THE FIRST SURFACE THAT CONSEQUENTLY ALSO CONNECTS THE INPUT TO ONE OF THE ANODES OF THE DIODE ARAY ON THE SECOND SURFACE. THE TERMINAL NODES OF THE INTEGRATED CIRCUIT WILL BE ORDINARY CMOS PADS, ACCESSIBLE ON THE FIRST SURFACE
DEPOSIT SENSOR MATERIAL ON SECOND SURFACE OF THE WAFER SO AS TO FORM AN ARRAY OF DIODES. EACH VIA OF THE SECOND SURFACE WILL CONNECT TO THE DIODE ARRAY IN ORDER TO FORM THE ANODES. THE TERMINAL NODES OF THE INTEGRATED CIRCUIT WILL BE ORDINARY CMOS PADS, ACCESSIBLE ON THE FIRST SURFACE
SCRIBE AND ENCAPSULATE TO FORM MODULAR SENSOR ARRAYS THAT CAN BE JUXTAPOSED EDGE TO EDGE
END

FIG. 12

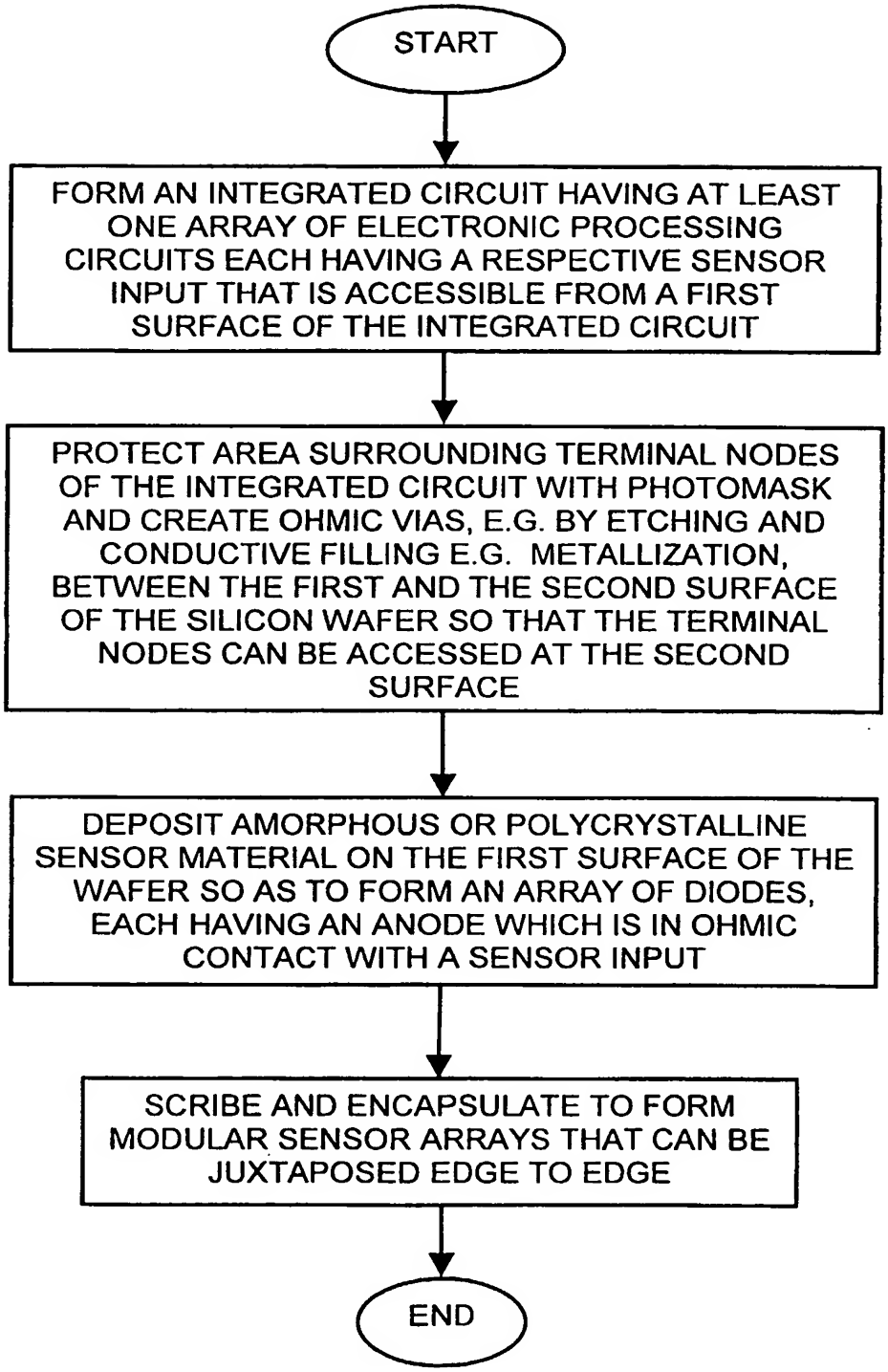
START
FORM AN INTEGRATED CIRCUIT HAVING AT LEAST ONE ARRAY OF ELECTRONIC PROCESSING CIRCUITS EACH HAVING A RESPECTIVE SENSOR INPUT THAT IS ACCESSIBLE FROM A FIRST SURFACE OF THE INTEGRATED CIRCUIT
PROTECT AREA SURROUNDING TERMINAL NODES OF THE INTEGRATED CIRCUIT WITH PHOTOMASK AND CREATE OHMIC VIAS, E.G. BY ETCHING AND CONDUCTIVE FILLING E.G. METALLIZATION, BETWEEN THE FIRST AND THE SECOND SURFACE OF THE SILICON WAFER SO THAT THE TERMINAL NODES CAN BE ACCESSED AT THE SECOND SURFACE
DEPOSIT AMORPHOUS OR POLYCRYSTALLINE SENSOR MATERIAL ON THE FIRST SURFACE OF THE WAFER SO AS TO FORM AN ARRAY OF DIODES, EACH HAVING AN ANODE WHICH IS IN OHMIC CONTACT WITH A SENSOR INPUT
SCRIBE AND ENCAPSULATE TO FORM MODULAR SENSOR ARRAYS THAT CAN BE JUXTAPOSED EDGE TO EDGE
END

FIG. 13

INTERNATIONAL SEARCH REPORT

Internati[illegible] Application No
PCT/IL 03/00125

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/06 H01L27/146 H01L31/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 254 868 A (SAITO YUTAKA) 19 October 1993 (1993-10-19) abstract; figures 2,3,13 column 2, line 52-65 column 3, line 26-28 column 6, line 12-20	1-3,6,7, 24
Y	---	8-13,15, 16
Y	US 5 998 292 A (BURGHARTZ JOACHIM NORBERT ET AL) 7 December 1999 (1999-12-07) column 3, line 59-66 column 4, line 3-7 column 5, line 22-33; figures 1,2,4	8-13,15, 16

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

'A' document defining the general state of the art which is not considered to be of particular relevance

'E' earlier document but published on or after the international filing date

'L' document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

'O' document referring to an oral disclosure, use, exhibition or other means

'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

'Y' document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 July 2003	31/07/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Cabrita, A

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 317 (E-449), 28 October 1986 (1986-10-28) -& JP 61 128564 A (FUJITSU LTD), 16 June 1986 (1986-06-16) abstract; figures 1A-1D figure 2	1-3,24
Y		17-19
Y	EP 1 045 450 A (AGILENT TECHNOLOGIES INC) 18 October 2000 (2000-10-18) column 6, line 9-27,43-50; figures 2,12	17-19
X	EP 0 537 514 A (MITSUBISHI ELECTRIC CORP) 21 April 1993 (1993-04-21) abstract column 1, line 19-24 column 4, line 35-40 column 6, line 50-53 figure 2 figures 3A-3E	1-3,24
X	US 4 547 792 A (SCLAR NATHAN) 15 October 1985 (1985-10-15) column 2, line 54-63; figures 6,7	1-3,24
A	US 4 857 746 A (KUHLMANN WERNER ET AL) 15 August 1989 (1989-08-15) abstract; figure 8	1-24

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internati(Application No
PCT/IL 03/00125

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5254868	A	19-10-1993	JP	3077034 B2	14-08-2000
			JP	4082267 A	16-03-1992
US 5998292	A	07-12-1999	TW	401611 B	11-08-2000
JP 61128564	A	16-06-1986	NONE		
EP 1045450	A	18-10-2000	US	6586812 B1	01-07-2003
			EP	1045450 A2	18-10-2000
			JP	2000340780 A	08-12-2000
			US	2003107100 A1	12-06-2003
EP 0537514	A	21-04-1993	JP	5110048 A	30-04-1993
			EP	0537514 A2	21-04-1993
			US	5357121 A	18-10-1994
US 4547792	A	15-10-1985	DE	3177014 D1	20-04-1989
			EP	0042604 A2	30-12-1981
			JP	57027054 A	13-02-1982
US 4857746	A	15-08-1989	DE	3633181 A1	07-04-1988
			JP	2557324 B2	27-11-1996
			JP	63102379 A	07-05-1988